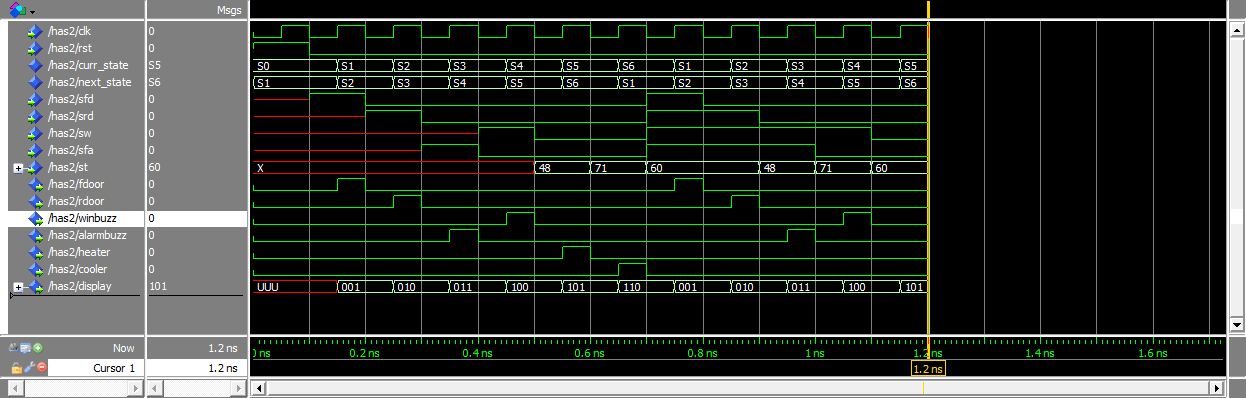
Team 8 VLSI Report

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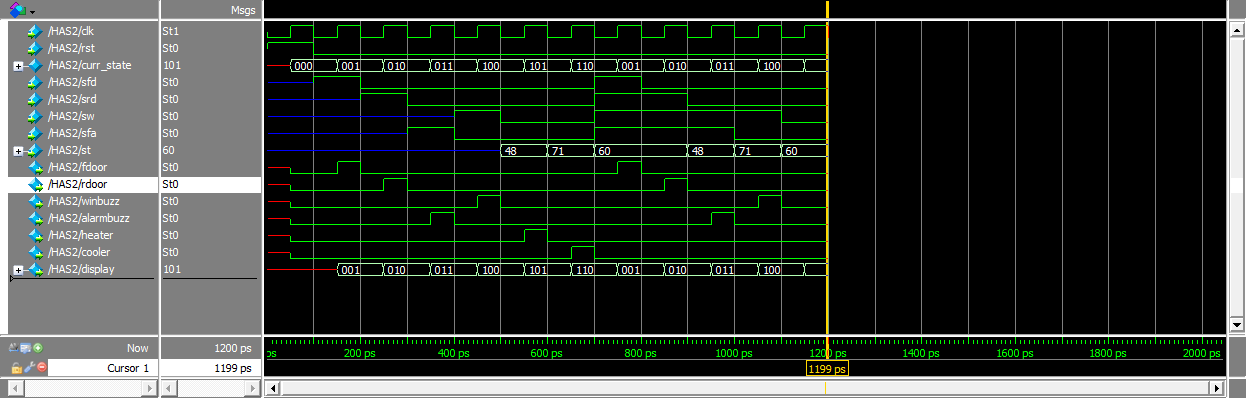
1. Diagram

   Description automatically generatedDiagram

   Description automatically generated
   1. Pre-Synthesis Simulation Screenshot
   2. Design Schematic After Synthesis Screenshot

Graphical user interface, diagram

Description automatically generated

* 1. Post-Synthesis Simulation Screenshot
  2. A screenshot of a computer

     Description automatically generatedChip Schematic Screenshot
  3. Table

     Description automatically generatedDesign
  4. Path

Table

Description automatically generated

* 1. Table

     Description automatically generatedPower

1. Justification
2. At first, we designed a circuit that handles priority, but it had problems with starvation. Our second design was implemented sequentially to deal with the starvation problem. The rationale behind using the sequential design is that through its simplicity, we can minimize our area and power consumption, and drive up the clock speed. This would make the delay between checking a signal in 2 rounds negligible while still not suffering from starvation. Simply, it’s a small, power efficient, and fast design.
3. Score

0.5 \* 68 + 0.3 \* (1500 – 670.9) + 0.2 \* (91.643) = **301.0586**